Kalinga University Atal Nagar (C.G.)

SCHEME OF EXAMINATION

& SYLLABUS

of

M.Tech Electronics & Telecommunication (VLSI Design & Embedded Systems)

UNDER

Faculty of Engineering and Technology

w.e.f. Session 2021-22

Kalinga University					
M.Tech Electronics & Telecommunication (VLSI Design & Embedded Systems)					
w.e.f 2021-22 session					
Semester -I					
Code No.	**Paper**	**Credits**	**End Semester Exam**	**Internal Marks**	**Total Marks**
MEVLSE101	CMOS Analog Circuit Design	4	100	50	150
MEVLSE102	Hardware Descriptive language	4	100	50	150
MEVLSE103	VLSI Technology	4	100	50	150
MEVLSE104	Advanced Microcontrollers & Embedded Systems Design	4	100	50	150
MEVLSE105	Programmable Logic Controller	4	100	50	150
MEVLSE106-P	Lab-I CMOS Circuit Design	1	30	20	50
MEVLSE107-P	Lab-II Advanced Microcontrollers & Embedded Systems Design	1	30	20	50
	Total	**22**	**560**	**290**	**850**
Semester - II					
Code No.	**Paper**	**Credits**	**End Semester Exam**	**Internal Marks**	**Total Marks**
MEVLSE201	Mixed Signal and RF Circuit Design	4	100	50	150
MEVLSE202	CMOS Digital circuit Design	4	100	50	150
MEVLSE203	Digital Signature Processor	4	100	50	150
MEVLSE204	Application Specific Integrated Circuits	4	100	50	150
Refer Below Elective – II		4	100	50	150
MEVLSE205A	Neural Network for VLSI				
MEVLSE205B	VLSI System Testing				
MEVLSE205C	ULSI Technology				
MEVLSE206-P	Lab-I CMOS Circuit Design	1	30	20	50
MEVLSE207-P	Lab-II DSP Processor	1	30	20	50
	Total	**22**	**560**	**290**	**850**

Semester - III					
Code No.	**Paper**	**Credits**	**End Semester Exam**	**Internal Marks**	**Total Marks**
MEVLSE301	ARM Processor and controller	4	100	50	150
MEVLSE302	Communication & Research Methodology	4	100	50	150
Refer Below Elective – III		4	100	50	150
MEVLSE303A	Algorithm for VLSI Design Automation				
MEVLSE303B	Electromagnetic Interference and Compatibility in system Design				
MEVLSE303C	VLSI signal processing				
MEVLSE304	Preliminary Work on Dissertation	9	100	50	150
MEVLSE305	Seminar Based on Dissertation	1	100	50	150
	Total	**22**	**500**	**250**	**750**
Semester - IV					
Code No.	**Paper**	**Credits**	**End Semester Exam**	**Internal Marks**	**Total Marks**
MEVLSE401-P	Dissertation	18	300	200	500
	Total	**18**	**300**	**200**	**500**

SEMESTER I

MEVLSE101

CMOS Analog Circuit Design

UNIT- I Basic MOS Device Physics & Layout Issues :-
MOS I/V Characteristics, MOS Device Models, Small-Signal Models of the MOS Transistors, Short-Channel Effects in MOS Transistors, CMOS Layout and Design Rules, Analog Layout Considerations, Latch-Up, ESD. **Y Chart for Circuit design**

UNIT –II Basic Current Mirrors and Single –Stage Amplifiers:-
Simple CMOS Current Mirror ,Common-Source Amplifier, Source-Follower or Common-Drain Amplifier, Common-Gate Amplifier, Source-Degenerated Current Mirrors, High-Output-Impedance Current Mirrors, Cascode Gain Stage, MOS Differential Pair and Gain Stage**. Frequency Response of amplifier**

UNIT – III Frequency Response and Noise:-
Miller Effect , Association of Poles with Nodes ,Frequency Response for Common Source, Source Follower ,Common Gate Stage, Cascode Stage & Differential Pair. **Noise:**-Types of Noise, Representation of Noise in Circuits, Noise in Single Stage Amplifiers, Noise in Differential Pairs, Noise Bandwidth.

UNIT- IV Advanced Current Mirrors, Op-amp Design & Compensation.:-
Advanced Current Mirrors, Folded-Cascode Op-amp, Current Mirror Op-amp, Fully Differential Op-amps, Common Mode Feedback Circuits Two Stage CMOS Op-amp, Feedback and Op-amp Compensation, Nonlinearity and Mismatch Issues for Differential Circuits. **Basic application of OPAMP**

UNIT – V Sample and Hold, Bandgap Reference, Switch-Capacitor Circuits:-
Performance of Sample and Hold Circuits, MOS Sample and Hold Basics, CMOS S/H Circuits, Bandgap Voltage Reference Basics, Circuits for Bandgap References, Switched–Capacitor Amplifiers, Switched Capacitor Integrator, Switched Capacitor Common Mode Feedback.

Text Books:-

1) B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2000. 2) D. A. Johns and K. Martin, Analog Integrated Circuit Design, Wiley, 1997. 3) P. Gray, P. J. Hurst, S. H. Lewis and R. Meyer
2) B.G. Streetman, "Solid State Electronics Devices", Prentice Hall.
3) Device Electronics for Integrated circuits by muller and kammins.

MEVLSE102 **Hardware Descriptive Language**

UNIT- I Introduction to VHDL:-
Basic concepts of hardware description languages. Hierarchy, Con currency, Logic and Delay modeling. Structural, Data-flow and Behavioral styles of hardware description.

UNIT- II Architecture of event driven simulators. Syntax and Semantics of VHDL. Variable and signal types, arrays and attributes. Operators, expressions and signal assignments. Entities, architecture specification and configurations. Component instantiation. Concurrent and sequential constructs. Use of Procedures and functions, Examples of design using VHDL.**Top to bottom approach of Circuit.**

UNIT- III Model simulation:- Simulation, Writing test bench, converting real and integer to time, Dumping result into text file, Reading vector from a text file, Test bench examples, Variable file names. **Text Bench Waveform**

UNIT-IV Hardware modeling examples:- Modeling entity interfaces, Modeling simple elements, Different types of modeling, Modeling regular structures, Modeling delays, Modeling conditional operations, Modeling synchronous logic, State machine Modeling, Interacting state machine, Modeling a Moore FSM, Modeling Mealy FSM, Generic priority encoder, Clock divider, Generic binary multiplier, Hierarchy in design.

UNIT- V verilog: Syntax and Semantics of Verilog. Variable types, arrays and tables. Operators, expressions and signal assignments. Modules, nets and registers, Concurrent and sequential constructs. Tasks and functions, Examples of design using Verilog. Synthesis of logic from hardware description.

Texts:
1. J. Bhaskar, "VHDL Primer", Pearson Education Asia 2001.
2. J. Bhaskar, "Verilog HDL Synthesis - A Practical Primer", Star Galaxy P
3) Fundamentals of Digital Logic with VHDL Design: Brown Vranesic, TMH Publication.
4) Synthesis and Optimization of Digital Circuits: Giovanni De Micheli, TMH Publication.
Reference Books
1) Circuit Design with VHDL Prdroni PHI Publication
2) VHDL Primer Bhaskar PHI Publication
3. Samir Palnitkar

MEVLSE103 VLSI Technology

UNIT-I: Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques. Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modeling, technology and damage annealing; characterization of Impurity profiles.

UNIT-II: Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films; High k and low k dielectrics for ULSI. Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

UNIT-III: Chemical Vapour Deposition Techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.**Different method of CVD**

UNIT-IV: Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallization schemes.**Different techniques of Metal Film Deposition**

UNIT-V: Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technologies**. Bi-CMOS Circuit**

Texts/References:

1. C.Y. Chang and S.M.Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.
2. S.K. Gandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.

Text Books

1. Jean Warland and Pravin Varaiya, " High Performance Communication Networks", 2nd edition,
2. Harcourt and Morgan Kauffman , London, 2000.
3. Willium Stalling , " Data and computer Communication"
4. **Referance Books**
5. 1)Leon Gracia, Widjaja, " Communication Networks", Tata McGraw

MEVLSE 104

Advanced Microcontrollers & Embedded Systems Design

UNIT I: Overview of microcontrollers: Architectures (functional block diagram only) of AT89c52, 89c51RD2, and 8096**. Difference between Microprocessor & Microcontroller**.

UNIT II: AVR Microcontrollers: Introduction to AVR microcontroller, Architecture of ATMEGA168, 8 bit microcontroller, GP registers, GP I/O ports, Instructions, Programming in Assembly language,.

UNIT III: ATMEGA168, 8 bit microcontroller Timers/Counters, PWM, Serial comm. USART**, RS232** signaling, Two wire interface I^2C, Serial peripheral Interface,

UNIT IV: **Interfacing and signaling :** interfacing between analog and digital blocks, signal conditioning, digital signal processing interfacing ADC, DAC, LCD with ATMEGA168, 8 bit microcontroller. **Introduction of CPLD & FPGA, Difference between PLA & PAL**

UNIT V: Aspects of embedded systems : Design trade offs due to process compatibility, thermal considerations, etc. Software aspects of embedded systems, Serial Communication Programming Using C for AT89c52.

Text Books:

1 John B Peat man " Design with Microcontroller ", Pearson education Asia, 1998.
2 Jonathan W. Valvano Brooks/cole “Embedded Micro computer Systems. Real time Interfacing ", Thomson learning 2001.
3 Steven f. Barret, Daniel pack, Mitchell Thorton, “Atmel AVR microcontroller primer, programming and interfacing”.
4 8051 Microcontroller and Embedded System 2nd edition by Mazidi

References:

1 David E Simon, " An embedded software primer ", Pearson education Asia, 2001.
2 Dhananjay Gadre, “ programming and customizing the AVR microcontroller”
3 J.W. Valvano, "Embedded Microcomputer System: Real Time Interfacing"

MEVLSE 105

Programmable Logic Controller

UNIT-I PLC Basics: Overall look at programmable Logic Controllers, General PLC Programming Procedure, Devices to which PLC Input and Output Modules are connected. Basic PLC Programming: Programming On/Off Inputs to Produce On-Off Outputs, Relation of Digital Gate Logic to Contact/Coil Logic.

UNIT-II Basic PLC Functions: Creating Ladder Diagrams from Process Control Descriptions, Register Basics, PLC Timer Functions, PLC Counter Functions. PLC Arithmetic Functions, PLC Number Comparison Functions.

UNIT-III Data Handling Functions: The PLC SKIP and MASTER CONTROL RELAY Functions, Jump Functions, PLC Data Move Systems, PLC Functions Working with Bits, PLC Digital Bit Functions and Applications, PLC Sequencer.

UNIT-IV Advanced PLC Functions and process control: Analog PLC Operation, PID Control of Continuous Process, Networking PLCs. PLC Control examples: Lift simulator, Bottling plant, Temperature control, Pneumatic and hydraulic plant, Machine control panel.

UNIT-V PLC installation and maintenance: PLC Auxiliary Commands and Functions, PLC installation, Troubleshooting and Maintenance, Selecting a PLC, Operation Simulation and Monitoring, Commonly Used Circuit Symbols.

Text Books:

1. Programmable Logic Controllers, John W. Webb, Ronald A. Reis; Prentice Hall - 5th Ed
2. Computer Based Industrial Control, Krishna Kant**;** Prentice Hall

Reference Books:

1. Programmable Logic Controllers: Principles & Applications, Webb & Reis, Prentice Hall of India.
2. Programmable Logic Control: Principles & Applications, NIIT, Prentice Hall of India.

SEMESTER II

MEVLSE 201

Mixed Signal and RF circuit Design

Unit I: Basic Concepts in RF design : Nonlinearity and Time Variance, Intersymbol Interference, RandomProcesses & Noise , Sensitivity & Dynamic Range, Passive Impedance Transformation, Passive RLC Networks ,Characteristics of Passive IC Components.

Unit II: **Distributed Systems:-** Link between Lumped and Distributed Regimes, Driving Point Impedance,Finite Length Transmission Lines, Smith Chart, S parameter , Bandwidth Estimation Techniques:-Method of Open-Circuit & Short –Circuit Time Constants.

Unit III: Low Noise Amplifier :- General Consideration ,Input Matching ,CMOS LNAs ,CMOS Mixers,Noise inMixers,Basic LC Oscillator Topologies, VCO,Phase Noise ,CMOS LC Oscillator ,Quadrature Signal Generation ,Single Sideband Generation.

Unit IV: Data Converters:- Specification of Converters,Flash Converter,Dual Slope A/D Converter, Pipelined& Sigma Delta Converter. D/A Converters, R-2R, Binary weighted ,Weighted Capacitor Converter System,Self Calibrating D/A Converter System.

Unit V: Frequency Synthesizers, Linearized PLL Models, Noise Properties of PLLs, Phase Detectors,LoopFilters ,Charge Pumps,RF Synthesizer Architecture, Frequency Divider.

Text Book:

1) T. H. Lee, Design of CMOS Radio Frequency Integrated Circuits, Second Edition, CUP, 2004.
2) R. J. van de Plassche, Integrated A-D and D-A Converters, Second Edition, Springer/Kluwer, 2003. (Cheap
Edition)
3) B. Razavi, *RF Microelectronics, IEEE Press.*

Reference:

1. B. Razavi, Monolithic Phase-locked Loops and Clock Recovery Circuits: Theory and Design, IEEE Press, 1996.
2. Baker, CMOS mixed signal circuit design.wiley eastern, ISBN 978-0-470-29026-2

MEVLSE 202

CMOS Digital Circuit Design

UNIT – I Basic Electrical Properties of MOS circuits: MOS transistor operation in linear and saturatedregions, MOS transistor threshold voltage, MOS switch and inverter, latch-up in MOS inverter; sheet resistance and area capacitances of layers, wiring capacitances;**Pull Up network & Pull Down Network**

UNIT – II CMOS inverter properties - robustness, dynamic performance, regenerative property, inverterdelay times, switching power dissipation, MOSFET scaling - constant-voltage and constant-field scaling;**Text Bench Wave form of CMOS Inverter**

UNIT – III Dynamic CMOS design: steady-state behavior of dynamic gate circuits, noise considerations indynamic design, charge sharing, cascading dynamic gates, domino logic, np-CMOS logic, problems in single-phase clocking, two-phase non-overlapping clocking scheme;

UNIT- IV Subsystem design: design of arithmetic building blocks like adders - static, dynamic, Manchestercarry-chain, look-ahead, linear and square-root carry-select, carry bypass and pipelined adders and multipliers - serial-parallel, Braun, Baugh-Wooley and systolic array multipliers,

UNIT – V Barrel and logarithmic shifters, area-time tradeoff, power consumption issues; designingsemiconductor memory and array structures: memory core and memory peripheral circuitry.**Different types of Power Deception in CMOS Circuit**

Texts:

1 J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits- A Design Perspective, 2nd Ed, PHI, 2003.
2 D. A. Pucknell and K. Eshraghian, Basic VLSI Design, PHI, 1995.
3 E. D. Fabricius, Introduction to VLSI Design, McGraw Hill, 1991.
4 Stephen Brown, "Fundamentals of digital design with VHDL design"

References:

1 N. H. E. Waste and K. Eshraghian, Principles of CMOS VLSI Design - a System Perspective, 2nd Ed, Pearson Education Asia, 2002.
2 S. M. Kang and Y. Leblevici, CMOS Digital Integrated Circuits Analysis and Design, 3rd Ed, McGraw Hill, 2003.
3 J. P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & Sons Pvt. Ltd, 2002.
4 W. Wolf, Modern VLSI Design - System on Chip design, 3rd Ed, Pearson Education, 2004.
1. R. Jacob *Baker, CMOS Circuit Design, Layout, and Simulation, IEEE Press, 1997.978-0-470-29026-2*

MEVLSE203

Digital Signal Processors

Unit I: Computational characteristics of DSP algorithms: basic DSP operations; a generic instruction-setarchitecture for DSPs; architectural requirement of DSPs: techniques for enhancing computational throughput - parallelism and pipelining;**FIR & IIR Technique**

Unit II: Data-path of DSPs: multiple on-chip memories and buses, dedicated address generator units,specialized processing units (hardware multiplier, ALU, shifter). On-chip peripherals for communication and control; control-unit of DSPs: pipelined instruction interrupts;

Unit III: Architecture of Texas Instruments fixed-point and floating-point DSPs: architecture ofTMS320C5x, C54x/C3x DSPs, Programmer's model, addressing modes, assembly language instructions; memory interfacing, parallel I/O interfacing; on chip peripheral: timer and serial port interface;

Unit IV: Description of TMS6xxx series; architecture of analog devices fixed-point and floating-point DSPs:brief description of ADSP 218x / 2106x DSPs; programmer's model; **Advanced DSPs:** TI's TMS 320C6x, ADI's Tiger-SHARC, Lucent Technologies' DSP 16000 VLIW processors;

Unit V: Multirate DSP: concept of multirate signal processing, Interpolation, Decimation, Filter formultirate, multirate DSP Application.

Texts

1. P. Pirsch, Architectures for Digital Signal Processing, John Wiley, 1999.
2. R. J. Higgins, Digital Signal Processing in VLSI, Prentice-Hall, 1990.
3. Analog Devices ADSP 2100-family and 2106x-family Users Manuals.
4. K. Parhi, VLSI Digital Signal Processing Systems, John Wiley, 1999.

References:

1. *K Parhi and T. Nishitani, Digital Signal Processing for Multimedia Systems, Marcel Dekker, 1999.*
2. *IEEE Signal Processing Magazine, Oct 88, Jan 89, July 97, Jan 98, March 98 and March 2000.*
3. *Texas Instruments TMSC5x, C54x and C6x Users Manuals*

MEVLSE 204

Application Specific Integrated Circuits

UNIT –I Introduction **to ASIC**, Modeling combinational and sequential circuits, Design entry by verilog / VHDL/FSM / SYSTEM C, Hardware modeling with Verilog / VHDL, different Verilog /VHDL constructs, and Logic Synthesis.

UNIT – II ASIC construction, Simulation ,Verification of complex logic design model, Verification issues likeverification plan, verification methodology, timing verification, Hardware design verification, Software design verification ,verification strategy for ASIC bus functional models,

UNIT – III verification Automation, physical verification, Layout planning and verifications ,ASIC designflow and HDL based ASIC design flow, EDA tools for ASIC design, Mixed signal design , Introduction to VLSI physical design, floor planning , placement and routing parameter extraction ,

UNIT – IV Analysis: static timing analysis , current analysis , clock tree synthesis , power grid analysis , clockskew analysis and post layout synthesis , Data structure for graph models, , different tools for the PAR, Design rule and electric rule checking, LVS , Wire length / load estimator, stick diagrams by using CMOS for various combination Ckt and Different timing parameters for ASICs.

UNIT V Test specification , need for testability, Boundary Scan Test , Faults , Fault simulation , AutomaticTest pattern Generation , SCAN test , Built in Self test ,Gate level simulation and IC verification. Tools used for front to back end chip design.

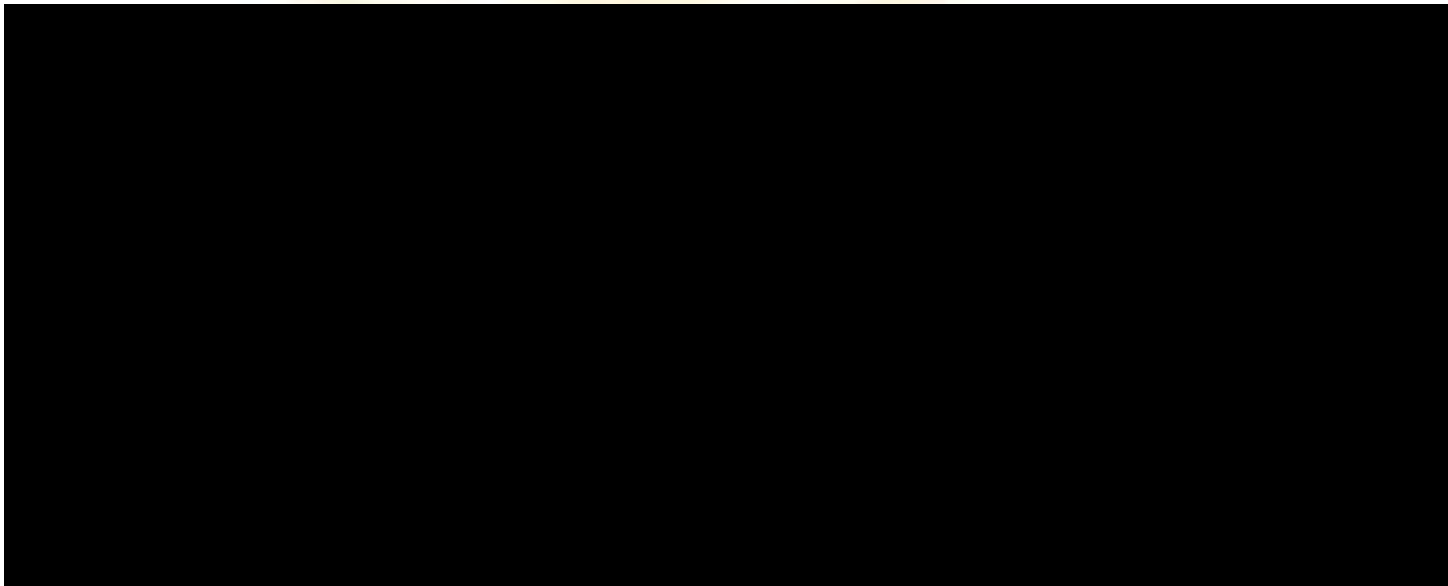
Text books:

1. Wayne Wolf, "Modern VLSI Design "byPearson Education Asia

2. Michael Smith,"Application Specific Integrated Circuits –"by Pearson Education Asia

References: .

1. Geiger, Allen Strader,"VLSI Design Techniques for Analog and Digital circuits "McGraw HILL
2. Neil Waste," Principles of CMOS VLSI Design "by Pearson Education Asia



MEVLSE205 A

Neural Networks for VLSI

UNIT I

Introduction: History, overview of biological Neuro-System, Mathematical Models of Neurons

UNIT II

ANN architecture, Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcementLearning.

UNIT III

Supervised Learning and Neurodynamics: Perceptron training rules, Delta, Back propagation trainingalgorithm, Hopfield Networks, Associative Memories.

UNIT IV

Unsupervised and Hybrid Learning: Principal Component Analysis, Self-organizing Feature Maps, ARTnetworks, LVQ

UNIT V

Applications for VLSI Design: Applications of Artificial Neural Networks to Function Approximation,Regression, Classification, Blind Source Separation, Time Series and Forecasting.

Text:

1. Anderson J.A., "An Introduction to Neural Networks", PHI, 1999

2. Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall International,
New Jersey, 1999.

Reference:

1. Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications andProgramming Techniques", Addison-Wesley, Reading, Mass, (1992).

2. Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge, MA, 1996.

3. Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York, 1998.

MEVLSE205B

VLSI System Testing

UNIT I

Special purpose Subsystems: Packaging, power distribution, I/O, Clock, Transconductance amplifier,follower integrated circuits, etc. **Design Economics:** Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Personpower, example

UNIT II

TESTING OF COMBINATIONAL CIRCUITS: Faults in digital circuits–Failures and faults–Modeling of faults–Temporary faults – Test generation for Combinational logic circuits – testable combinational logic circuit design – Scan based design and JTAG testing issues.**Error detecting Technique of Circuit using 0 & 1**

UNIT III

TESTING OF SEQUENTIAL CIRCUITS: Test generation for sequential circuits–Design of testable sequentialCK5- Built in self test – Testable memory design.

UNIT IV

VERIFICATION AND TESTING: Verification–Timing verification–Testing concepts–Fault coverage–ATPG–Types of tests – Testing FPGAs – Design for testability.

UNIT V

VLSI System Testing & Verification: Introduction, A walk through the Test Process, Reliability, LogicVerification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan. **VLSI Applications:** Case Study: **RISC microcontroller& CISC Microcontroller**, ATM Switch, etc.

Text:

1. Neil H.E. Weste, Davir Harris, "CMOS VLSI Design: A Circuits and system perspectives" Pearson Education 3rd Edition.
2. Wayne, Walf, "Modern VLSI design: System on Silicon" Pearson Education, Second Edition

References:

1. Pucknull, "Basic VLSI Design" PHI 3rd Edition

MEVLSE205C

ULSI Technology

Unit I :

Clean room Technology : Classification, Design concepts, **Introduction of LSI, MSI, LSI, & VLSI Technology**Installation, Operation and Automation.Wafer- Cleaning Technology**:** Basic concepts, Wet-Cleaning and Dry-Cleaning Technology. Epitaxy:Fundamental Aspects, Conventional Si Epitaxy, Low temperature Epitaxy of Si**, Selective Epitaxial Growth of Si.**

Unit II :

Conventional and Rapid thermal process: Requirement of thermal process, Rapid thermalprocessing, **Dielectric and polysilicon film deposition:** Deposition process, APCVD & LPCVD silicon oxides, LPCVD silicon nitride, LPCVD Polysilicon film, Plasma assisted Deposition, **Applications of deposited polysilicon, silicon oxide.**

UNIT III :

Lithography and Etching: Optical, Electron, X-ray , Ion lithography, Low pressure gas discharge,Etching mechanism, selectivity and profile control, Reactive plasma etching techniques and equipments, Plasma processing, Wet chemical etching. **Metallization:** Metal deposition technique, silicide process, CVD Tungsten plug and other plug process, Multilevel Metallization, Metallization Reliability,

UNIT IV:

Process integration: Basic process module and devices consideration for ULSI, CMOS Technology,Bipolar technology, BiCMOS technology, MOS memory technology, Process integration consideration in ULSI Fabrication Technology. **Assembly & Packaging:** Package type, ULSI assembly technology, Package fabrication technology, package design consideration, Special package consideration.**Packaging style IC**

UNIT V:

Wafer Fab Manufacturing technology: Wafer Fab manufacturing consideration, manufacturingstart-up technology, Volume ramp up Consideration, Continuous improvement. **Reliability:** Hot carrier injection, electromagnetism, stress migration, oxide breakdown, Effect of scaling on device reliability, Relation between DC and AC lifetime, Some recent ULSI Reliability concern, Mathematics of Failure distribution.

TEXT BOOK:

1. C.Y. Chang and S. M. Sze “ULSI Technology” McGraw-Hill publications.
2. Chen, “VLSI Technology” Wiley, March 2003.

REFERENCE BOOKS:

1. B.G. Streetman, “Solid State Electronics Devices”, Prentice Hall, 2002.
2. Sze, “Modern Semiconductor Device Physics”, John Wiley & Sons, 2000

MEVLSE206-P

CMOS Circuit Design Lab-I

Name of Experiments

1. Design and simulation of Common Source Amplifier.
2. Design and simulation of CMOS Inverter.
3. Design and simulation of Current Mirror.
4. Design and simulation of first stage of Opamp.
5. To draw layout of CMOS inverter
6. To draw layout of CMOS NAND gate.
7. To draw layout of CMOS NOR gate.
8. To draw layout using interdigitized and Common Centroid Method.
9. To draw layout of Resistance for a specific value.
10. To draw layout of Capacitor for a specific value..
11. To draw layout of a Differential amplifier.
12. To draw layout of a Current Mirror.

Note: Minimum 10 Experiments to be performed.

Extra experiments can be added if necessary.

MEVLSE207-P

DS Processor Lab-II

Lab Experiments

1. Design. of 16 bit adder & implementation using TMS 320C6X.
2. Design. of Algorithm to move a block from memory to register.
3. Design. & Implementation of a hardware multiplier using C Language programming.
4. Study of pipe line instruction use in processing of data with the help of interrupts.
5. Design. & Implementation of butter worth digital IIR filter by bl linear transformation method using TMS 320 C6 X.
6. Design. Of chebeshev Digital IIR filter using bi linear transformation with TMS 320C6X.
7. Design. Of FIR Digital filter by hanning or hamming window with the help of TMS 320C5X / C6X.
8. Write on Algorithm to implement & process a filter speech signal at required frequency using any Digital Signal Processor.
9. Write on assembly language code to control stepper motor by standard Digital Signal Processor.
10. Write an algorithm to implement a simple diameter & Interpolator using standard Digital Signal Processor.

Note: Minimum 10 Experiments to be performed.

Extra experiments can be added if necessary.

Semester-III

MEVLSE301

ARM Processor and controller

UNIT I

Introduction to 16 / 32-bit Micro controllers: ARM 7/ARM 9 architecture, ARM Microcontrollers and Processor Cores, ARM Architecture and Organization, ARM/THUMB Programming Model, ARM/THUMB Instruction Set , ARM Exception Handling ,More ARM Instructions, ARM/THUMB Assembly Programming

UNIT II

Data handling, interfacing with Memory, Interrupts, Timers, ARM Bus. I/O Devices, Controllers, Simple & Autonomous I/O Controllers,

UNIT III

Parallel, Multiplexed, Tristate, and Open-Drain Buses, Bus Protocols, Serial Transmission Techniques & Standards, Wireless protocols CAN & advanced Buses.

UNIT IV

Design Methodology, Design Flow, Architecture Exploration, Functional Design, Functional Verification, Synthesis, Physical Design,

UNIT V

Design Optimization, Area Optimization, Timing Optimization, Power Optimization, Design for Test , Fault Models and Fault Simulation, Scan Design and Boundary Scan, Built-In Self Test (BIST), Nontechnical Issues.

BOOKS

1. *Data books of ARM7/ARM9 J. Staunstrup and W. Wolf, editors, Hardware/Software Co-Design: Principlesand Practice, Kluwer Academic Publishers, 1997.*

Reference:

1. ARM System-on-Chip Architecture, by Steve Furber ,Pearson Education **Edition:** 2nd

2. *Arm System Developer'S Guide: Designing And Optimizing System Software (Paperback)* by SlossAndrew N. Et.Al, **Publisher:** Morgan Kaufmann Publishers **Edition:** 1st

MEVLSE302

Communication and Research Methodology

Unit 1

Concepts of Communications: Definition, Forms of Communication, Objectives of Communication, Characteristics of Communication, Process of Communication, Communication, Roadblocks, Role of Verbal and Non-verbal Symbols in Communication, Barriers to Effective Communication, Overcoming Communication Barriers.

Nonverbal communication: Body Language, Gestures, Postures, Facial Expressions, Dress codes; the Cross Cultural Dimensions of Business Communication; Listening and Speaking, techniques of electing response, probing questions, Observation. Business and social etiquettes;

Listening Skills: Definition, Anatomy of poor Listening, Features of a good Listener, Role Play, Group Discussion and Interviews, Meetings: Ways and Means of conducting meetings effectively, Mock Meetings and Interviews

Unit 2

Reading and language skills: The reading process, purpose, different kinds of texts, reference material, scientific and technical texts, active and passive reading, strategies - vocabulary skills, eye reading and visual perception, prediction techniques, scanning skills, distinguishing facts and opinions, drawing inferences and conclusions, comprehension of technical material - scientific and technical texts, instructions and technical manuals, graphic information.

Forms of Communication in Written mode: Basics Body language of Business Letters and Memos, Tone of writing,

Enquiries, orders and replying to them, sales letters, Job applications and resume, E-mail: How to make smart e-mail, Writing Business Reports and Proposals, Practice for Writing.

Unit 3

Referencing and Writing skills: Business letters: Enquiries, Circulars, Quotations, Orders, Acknowledgments, Executions, Complaints, Claims and adjustments, Collection letter, Banking correspondence, Agency correspondence, Bad news and persuading letters, Sales letters, Job application letters - Biodata, Covering Letter, Interview Letters, Letter of Reference, Memos, minutes, Circulars & notices.

Types of Business Reports - Format, Choice of vocabulary, coherence and cohesion, paragraph writing, organization reports by individual, Report by committee.

Unit 4

Introduction to Research and Research Design: Nature and scope of research, information based decision making and source of knowledge. The research process; basic approaches and terminologies used in research. Defining research question and framing of hypotheses, preparing a research plan, qualitative and quantitative research designs, Experimentation, Observational studies, Exploring secondary data.

Measurement and Scaling, Data Source and Data Collection Field research: primary data collection from observations, surveys and experimentation. Measurement and scaling; commonly used scales in reliability and validity of scales. Designing instrument for data collection; testing the instrument, data collection process, Sampling methods and procedures and sample size decisions.

Unit 5

Data Analysis and Presentation Editing and coding of data, tabulation, graphic presentation of data, cross tabulation, Testing of hypotheses; type I and II errors, one tailed and two tailed tests of significance, Parametric and nonparametric tests for Univariate and Bivariate data. Tests of association; simple linear regression and other non parametric tests.

Technical Writing: Technical Proposal writing: Definition, Purpose, types, characteristics, Elements of structure, style and appearance, evaluation, exercises, Research report writing, Proposal writing, referencing, forms of reports, bibliography, etc. Research paper, Dissertation, and Thesis, Instruction Manuals, Type of instructions, Writing Instructions, Technical Descriptions, Process descriptions, Guidelines for Writing Good Descriptions.

Text Books:

1. Lesikar, R. V. & Flatley, Basic Business Communication Skills for Empowering the Internet Generation. TMH.
2. Meenakshi Raman, Sangeeta Sharma, Technical Communications, Oxford Latest Edition.
3. D. K. Bhattacharyya, Research Methodology, Excel Books 2nd Edition.

Reference Books:

1. Bowman, J.P. &Branchaw, P.P. Business Communications, Process to Product Dryden Press, Chicago.

MEVLSE303A

Algorithm for VLSI Design Automation

UNITI

Logic synthesis & verification: Introduction to combinational logic synthesis, Binary Decision Diagram,Hardware models for High-level synthesis.

UNIT II

VLSI automation Algorithms: Partitioning: problem formulation, classification of partitioning algorithms,Group migration algorithms, simulated annealing & evolution, other partitioning algorithms. Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor plannning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT III

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm,line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

UNIT IV

Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms,two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

UNIT V

Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained viaminimization. Compaction: problem formulation, one-dimensional compaction, two dimension-based compaction, hierarchical compaction, **Design Rule Check Concept**

Text:

5 Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

2.Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

References:

5. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP,2002.

6. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition

MEVLSE303B

Electromagnetic Interference and Compatibility in system Design

UNIT 1

EMI Environment

Sources of EMI conducted and radiated EMI, transient EMI, EMI-EMC definitions and units of parameters.

UNIT 2

EMI Coupling Principles

Conducted, radiated and transient coupling, common independence ground coupling, radiated common mode and ground loop coupling, radiated differential mode coupling, near field cable to cable coupling, power mains and power supply coupling.

UNIT 3

EMI Specification/Standards & Measurements

Unit of specifications, civilian standards military standards. EMI test instruments/systems, EMI test, EMI Shielded chamber, open area test site, TEM Cell antennas, conductors injectors/couplers, military test method and procedures, calibration procedures.

UNIT 4

EMI Control Techniques

Shielding, filtering, grounding, bonding, isolation transformer, transient suppressors, cable routing, signal control, component selection and mounting.

UNIT 5

EMC Design of PCBs

PCB traces cross talk, impedance control, power distribution decoupling, zoning, motherboard designs and propagation delay performance models.

Books:

1. *Bernhard Keiser, "Principles of ElectromagneticCompatibility", Artech house, 3rd Ed., 1986.*

Reference:

1. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", John wiley and Sons. 1988.

MEVLSE303C

VLSI Signal Processing

UNIT 1
Introduction to DSP systems – Iteration Bound – Pipelined and parallel processing.

UNIT 2
Retiming – unfolding – algorithmic strength reduction in filters and transforms.

UNIT 3
Systolic architecture design – fast convolution – pipelined and parallel recursive and adaptive filters.

UNIT 4
Scaling and round off noise – digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic.

UNIT 5
Numerical strength reduction – synchronous, wave and asynchronous pipe lines – low power design – programmable digit signal processors.

Book:

4. *Keshab K. Parthi, "VLSI Digital signal processing systems, design and implementation", Wiley, Inter Science, 1999.*
5. *Mohammad Isamail and Terri Fiez, "Analog VLSI signal and information processing", Mc Graw – Hill*
6. *S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.*

Reference:

7. *Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994*

MEVLSE304

Preliminary work on Dissertation

The student will submit a synopsis at the beginning of the semester for approval from the departmental committee in a specified format. The student will have to present the progress of the work through seminars and progress reports.

MEVLSE305

Seminar Based on Dissertation

The student will deliver a seminar on the topic chosen by him and approved by Departmental committee for evaluation at the end of semester

Semester-IV

MEVLSE401

Dissertation

The student will submit a detailed Project Report on the topic approved by Departmental committee i